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10/761,343	01/22/2004	Alex L. Chan	ALC 3113	3273

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KRAMER & AMADO, P.C.
Suite 240
1725 Duke Street
Alexandria, VA 22314

EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	**PAPER NUMBER**
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,343	CHAN ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3pg.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

1. Applicant's election with traverse of group I, claims 1-12, in the reply filed on 1/3/07 is acknowledged. The traversal is on the ground(s) that the Examiner has not fulfilled his burden of proving that these pending claims of the patent are either independent or distinct.

The argument is not persuasive. The distinct between two groups is that claims 1-12 drawn to a structure of a PCB while claim 13 drawn to a method of mounting a decoupling capacitor. The burden is that a prior art reference(s) may contain every limitation of the circuit board structure of group I (claims 1-12) but may not contain the method of group II (claim 13) or even not containing any method at all. Thus, a further search is required for just the method alone and this is the burden.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Objections

2. Claims 2-12 are objected to because of the following informalities:

Claim 2: On line 12 of the claim, the "via column C(n+1)" must be changed to -- via column Col(n+1) --.

Claim 2: For consistency, on line 13 of the claim, , the "column Col(n)" must be changed to -- via column Col(n) --, and "rows R(k)" must be changed to -- via rows R(k) --.

Claims 5-10: For consistency, the "column Col(n)" must be changed to -- via column Col(n) --, and "row R(k)" must be changed to -- via row R(k) --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the limitation "a modified vias array, the modification being that at least a portion of one row of said vias array is missing at least two adjacent vias, wherein the missing vias have been replaced by respective shared vias in an adjacent row, and said shared vias have been connected to either a power supply or a power return" is not complied with enablement requirement. The Examiner does not know how a portion of one row of vias array is missing at least two adjacent vias, and then the missing vias have been replaced by respective shared vias in an adjacent row. The missing vias are in a row (one row), then how these same missing vias are replaced by shared vias in adjacent row (the adjacent row leading to two rows, because two vias are in adjacent row must be located in two rows).

For continuing examination, the Examiner assumes that the applicants mean at least a portion of one **column** of said vias array is missing at least two adjacent vias. Then, the missing vias have been replaced by respective shared vias in an adjacent row is more reasonable.

Regarding claim 2, because the applicants fail to limit (or clearly define) the "n", "k", and "m", therefore the Examiner is confused by the limitations stated in the claim.

For example, the Examiner has assumed n=3, k=3, m=1 resulting an array of 3 via columns Col(1), Col(2), Col(3) corresponding to 3 via rows R(1), R(2), R(3), and 4 columns of none-via c(1), c(2), c(3), c(4) corresponding to 4 rows of none-via r(1), r(2), r(3), r(4). Then the limitation "2m corresponding vias in a via column Col(n+1) adjacent to via column Col(n) and placed in the successive via rows R(k) to R(k+2m-1) of said vias array are shared vias" resulting 2 corresponding vias in a via column Col(4) adjacent to via column Col(3) and placed in the successive rows R(3) to R(4) of the vias array are shared vias. In this example, the Examiner does not know where to place the 2 shared vias, since the last via column is Col(3) and the last via row is R(3).

Examiner remarks: Regarding claims 2-10, it seems more reference characters are needed in regarding a via column or a via row within an (n) number of via columns and a (k) number of via rows. For example, via column col("i"), where "i" is greater than 1 and smaller than "n", where "n" in the number of via columns.

For continuing examination, the Examiner assumes the limitations "wherein 2m vias of said via column Col(n) placed in successive via rows R(k) to R(k+2m-1) of said modified vias array are depopulated to obtain a free space on the back side of said PWB, and wherein 2m corresponding vias in a via column C(n+1) adjacent to said column Col(n) and placed in said successive rows R(k) to R(k+2m-1) of said vias array are shared vias"

means:

"wherein 2m vias of via column Col(i) of said via columns Col(n) placed in successive via rows R(j) to R(j+2m-1) of said via rows R(k) of said modified vias array are depopulated to obtain a free space on the back side of said PWB, and

wherein 2m corresponding vias in a via column Col(i +1) adjacent to said via column Col(i) and placed in said successive rows R(j) to R(j+2m-1) of said vias array are shared vias; and, wherein i<n and j<K".

Regarding claims 5-10, the Examiner is also confused by the limitation "shared via in said via column Col(n)" in the claims. As disclosed in claim 2, the claim stated that the shared vias are in Col(n+1), but now claims 5-10 restated that the shared vias are in Col(n). The Examiner does not know which via column that claims 5-10 indeed refer to.

For continuing examination, the Examiner assumes that the applicants mean via column Col(i+1) instead of "column Col(n)", c(i+1) instead of c(n), and c(i+2) instead of c(n+1). It is noted Col(i) is in between c(i) and c(i+1), thus if a via is in Col(i+1) then its pads are in c(i) and c(i+2). And, in responding to the assumption as discussed in claim 2 above, all references (n) and (k) are considered as (i) and (j) in referring to an individual column and row within the via array having (n) number of columns and (k) number of rows.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Clarkson et al. (US 20030043560, hereafter Clarkson).

Regarding claim 1, at least as shown in figures 2A-4B, Clarkson discloses a printed wiring board for mounting a high performance ball grid array (BGA) device on one side of the PWB comprising:

(a) a modified vias array (circular shapes as shown in the figures, see figure 2 for example),

(b) the modification being that at least a portion of one column of vias array (considering column 4 from left, figure 2A for example) is missing at least two adjacent vias (arbitrarily selecting any two vias in column 4), wherein the missing vias have been replaced by respective shared vias in an adjacent row (see figure 4B, paragraph 30, ground/power vias and decoupling capacitors), and the shared vias have been connected to either a power supply or a power return (par.30)

(c) a via pad (square shapes as shown in the figures) for each shared vias (every via has a via pad) located on the other side of the PWB in the portion,

(d) whereby a decoupling capacitor (no reference number, see figures 4A-B, capacitors are mounted to power and ground vias, see paragraph 30) can be electrically connected across the pair of via pads to decouple the power supply and the power return at the two adjacent vias.

Regarding claim 2, at least as shown in figures 2A-4B, Clarkson discloses a printed wiring board (PWB) for mounting a high performance integrated circuit, comprising:

(a) on a top side of the PWB (figure 4A for example), a modified via array with BGA columns and BGA rows of ball connection pads (see figures 2A-B for clearer illustration of vias and pads);

(b) a modified vias array of plated through hole vias (see par.18, columns 180-187), with each via column Col(n) arranged between two respective BGA columns c(n) and c(n+1) and each via row R(k) arranged between two respective BGA rows r(k) and r(k+1),

wherein 2 vias (considering m=1) of the via column Col(5) placed in successive via rows R(5) to R(6) of the modified vias array are depopulated (removed vias, see channel 130/135 in figures 2A-2B for example and par. 25) to obtain a free space on the back side of the PWB, and

wherein 2 corresponding vias (considering m=1) in a via column C(6) adjacent to column Col(5) and placed in the successive rows R(5) to R(6) of the vias array are shared vias (ground and power vias, see par.30).

Examiner remarks:

The Examiner considers each column and row vias Col(n) and K(n) are formed in between column and row of non-vias c(n), c(n+1), r(k), and r(k+1). For illustration purpose, figures 2 shows 9 columns and 9 rows of vias (n=k=9), in which column via Col(i=5) and row via R(i=5) are removed.

Regarding claim 3, as shown in figures 2A-2B, Clarkson discloses the free space has a width D1 equal to twice the pitch D of the vias array less a via size (clearly shown in the figures, also see par. 27), for accommodating 1 passive elements of a substantially similar width D1 (see par. 30).

It is noted that the limitation "for accommodating m passive elements of a substantially similar width D1" is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art. Furthermore, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ 2d 1647 (1987).

Regarding claim 4, Clarkson discloses m is at least one.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarkson.

Regarding claims 11 and 12, Clarkson discloses every limitation as shown in claim 3 above, but fails to disclose the passive elements are 0603, 0402, 0201 or smaller decoupling capacitors/resistors.

The Examiner takes Official notice that a selection of the type of passive component and its sizes is only a matter of design choice depending upon particular applications.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select either decoupling capacitors or resistors in the sizes of 0603, 0402, 0201 or smaller in order to meet a specific requirement of a particular application.

Allowable Subject Matter

9. Claims 5-10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Reasons for allowance

10. The following is an examiner's statement of reasons for allowance:

(a) **Regarding claim 5**, the best prior art reference, Clarkson et al. (US 20030043560), fails to teach or fairly suggest, a first shared via in the via column Col(6) and the via row R(5) provides a power contact to a first associated ball contact pad in the column c(6) and the row r(5) and to a second associated ball contact pad in the column c(7) and the row r(5). None of the reference art of record discloses or renders obvious such a combination.

(b) **Regarding claim 7**, the best prior art reference, Clarkson et al. (US 20030043560), fails to teach or fairly suggest, a first shared via in the via column Col(6)

and the via row R(5) provides a power contact to a first associated ball contact pad in the column c(6) and the row r(5) and to a second associated ball contact pad in the column c(6) and row r(6). None of the reference art of record discloses or renders obvious such a combination.

(b) **Regarding claim 9**, the best prior art reference, Clarkson et al. (US 20030043560), fails to teach or fairly suggest, a first shared via in the column Col(6) and the row R(5) provides a power contact to a first associated ball contact pad in the column c(6) and said row r(6) and to a second associated ball contact pad in the column c(7) and row r(6). None of the reference art of record discloses or renders obvious such a combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Citation of Relevant Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Osburn et al. (US 20040061241) disclose a semiconductor device power interconnect striping.

Cornelius et al. (US 6834427) disclose a method for depopulating of a ball grid array to allow via placement.

Degani et al. (US 6175158) disclose an interposer for recessed flip-chip package.

Gottschall. et al. (US 6037677) disclose a Dual-pitch perimeter flip-chip footprint for high integration asics.

Kwong et al. (US 20040099440) disclose a Technique for accommodating electronic components on a multiplayer signal routing device.

Miller et al. (US 20030183419) disclose a Ball assignment for ball grid array package.

Wyrzykowska et al. (US 20040216916) disclose a Technique for improving power and ground flooding.

Duxbury et al. (US 20040003941) disclose a Technique for electrically interconnecting electrical signals between an electronic component and a multilayer signal routing device.

Wyrzykowska et al. (US 20040040744) disclose a Technique for reducing the number of layers in a multilayer circuit board.

Katz (US 6594811) discloses a Routable high-density interfaces for integrated circuit devices.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoa C. Nguyen

Dean A. Reichard

DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

6/7/07